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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/080,657 | 02/25/2002 | Yoshihiro Ariyama | 32014-178508 | 1714 |
| 7590 | 06/09/2004 | | EXAMINER | |
| Venable P.O. Box 34385 Washington, DC 20043-9998 | | | SINGH, RAMNANDAN P | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2644 | |
| DATE MAILED: 06/09/2004 | | | | |

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | |
|------------------------------|-----------------------------|--------------------|
| Office Action Summary | Application No. | Applicant(s) |
| | 10/080,657 | ARIYAMA, YOSHIHIRO |
| | Examiner Ramnandan Singh | Art Unit 2644 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 18 March 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,2,5-8,11 and 12 is/are rejected.
- 7) Claim(s) 3,4,9 and 10 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 18 March 2004 have been considered but are moot in view of the new ground(s) of rejection.

2. **Status of Claims**

Claims 1, 3-7, 9-12 are amended.

Claims 1-12 are pending.

3. **Change of Scope**

With the amendment to the claims, a new search for prior art is necessitated. Thus , the new ground(s) of rejection are made.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-2, 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hasegawa [US 6,035,312] in view of Berger et al [US 4,679,166].

Regarding claim 1, Hasegawa teaches an echo canceller 120 having n

taps for generating an echo replica $\hat{y}(t)$ and for subtracting the echo replica from a local input signal $y(t)$ to create a residual signal $e(t)$ for outgoing transmission shown in Fig. 1, comprising:

a plurality of processors (i.e. **m filter circuits with $m < n$**) for generating the echo replica , $\hat{y}(t)$ [col. 4, lines 29-38]; and

a controller 106 coupled to the processors (i.e. **filters**) for grouping the filter coefficients into a plurality of segments (i.e. **performing selection or exchange of blocks**), evaluating (i.e. **monitoring**) information about the filter coefficients of the filter circuits [col. 4, lines 42-47], assigning the local input signal, $x(t)$, into the processors (i.e. **filter circuits**) [col. 1, lines 11-15; Figs. 1-5; col. 4, line 52 to col. 7, line 49].

Although Hasegawa teaches using a plurality of processors (i.e. filters) in parallel, he does not teach expressly processors having different computational accuracy.

Berger et al teach a dual-processor (i.e. **$m = 2$**) system , comprising: two parallel processors , an 8-bit processor , CPU 10, and a 16-bit processor , CPU 20 [Fig.1; col. 2, line 64 to col. 3, line 12], wherein the 8-bit processor is assigned to one set of tasks and the 16-bit processor to another set of tasks [col. 1, lines 22-27]. Thus, these two parallel processors have different computational accuracy. It may , however, noted that assigning different sets of tasks to individual processors depends on a specific application.

Hasegawa and Berger et al are analogous art because they are from a similar problem solving area, viz. , parallel processing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the dual processor system of Berger et al with Hasegawa.

The suggestion/motivation for doing so would have been to provide a multi-processor system wherein a plurality of processors cooperate in the performance of system tasks [Berger et al; col. 2, lines 59-64].

Claim 7 is essentially similar to Claim 1 and is rejected for the reasons stated above apropos of claim 1.

Regarding claim 2, Hasegawa further teaches computing a power of the coefficients for each of the segments (i.e. **blocks**) for selecting a maximum power block and a minimum power block [See Figs. 1 and 2].

Claim 8 is essentially similar to Claim 2 and is rejected for the reasons stated above apropos of claim 2

6. Claims 5-6 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hasegawa and Berger et al as applied to claims 1 and 7 above, and further in view of Ahamed et al [US 5,978,831].

Regarding claim 5, Hasegawa does not teach a (system) supervisor for monitoring a computational overflow for each segment and ordering the controller 106 to assign the local input signal to the processor.

Ahamed et al teach a supervisor (i.e. **system controller**) for a multi-processor system (Fig. 10) [col. 1, lines 31-47] for processor having different performance characteristics [col. 2, lines 9-29], wherein the supervisor provides high-level control over a multi-processor system for controlling a computation overflow (i.e. **inter-processor task distribution**) [col. 3, line 50 to col. 4, line 9; Fig. 10; col. 9, line 4 to col. 10, line 32; col. 13, lines 5-32].

Hasegawa, Berger et al and Ahamed et al are analogous art because they are from a similar problem solving area, viz. , parallel processing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the supervisor of Ahamed et al with the Hasegawa and Berger et al system.

The suggestion/motivation for doing so would have been to provide effective supervision (i.e. **system control**) over the multi-processing system in the performance of the systems tasks [Ahamed et al; col. 1, lines 34-46; col. 1, lines 12-13].

Claim 11 is essentially similar to Claim 6 and is rejected for the reasons stated above apropos of Claim 5

Claims 6 and 12 are similar to claim 5 and are rejected for the reasons stated above.

Allowable Subject Matter

7. Claims 3-4 and 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claim 3 claims identifies the uniquely distinct feature of the parallel processing comprising a controller that assigns the local input signal to the processor for higher computational accuracy when the power of each one of the segments is above a predefined threshold. While the closest prior art, Hasegawa [US 6,035,312], Berger et al [US 4,679,166, and Ahamed et al [US 5,978,831] each teach parallel processing using a set of processors, Hasegawa using a set of parallel filters, Berger et al using a

dual processor system, and Ahamed et al using a plurality of parallel processors; none of them suggest assigning the local input signal to the processor for higher computational accuracy when the power of each one of the segments is above a predefined threshold. As such, the prior art, either singularly or in combination fail to anticipate or render the above underlined limitation obvious. Therefore, claim 3 is objected to.

Claim 9 is essentially similar to claim 3 and hence claim 9 is also objected to.

Claims 4 and 10 are also objected for the reasons stated above.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ramnandan Singh whose telephone number is (703)308-6270. The examiner can normally be reached on M-F(8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester Isen can be reached on (703)-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2644

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ramnandan Singh
Examiner
Art Unit 2644

